**Design and implementation of XNOR gate**

**Objectives:**

The objective of this experiment is to learn designing and simulation of digital circuits at the transistor level using Verilog file and find the output of these circuit as a timing diagram. It can solve all type gate and easily solve the mathematical problems.

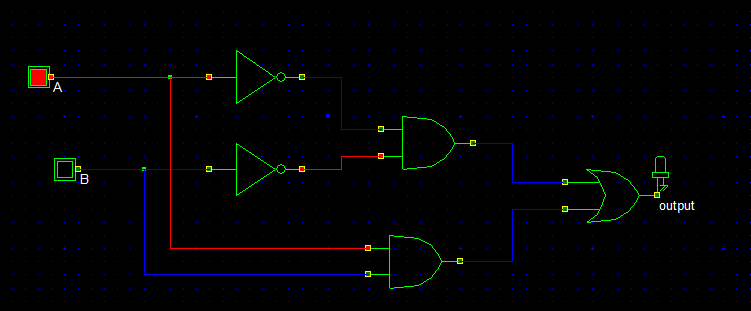
**Theory:**

A XNOR (Exclusive Nor) gate is a digital logic gate with two or more inputs such as input(A,B) and find a single output such as (Y). The XNOR gate will be true if the all input is true or all input is false, otherwise it will be false.

Truth Table:

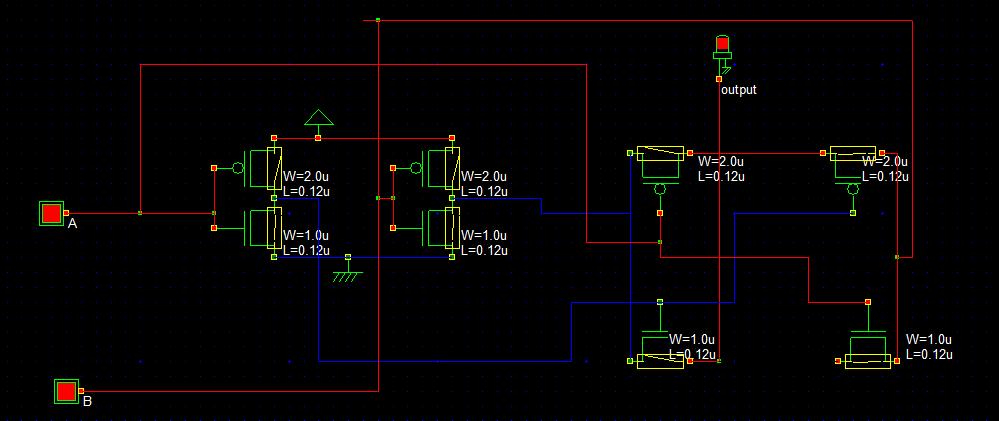
|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Circuit Diagram using the basic gate**

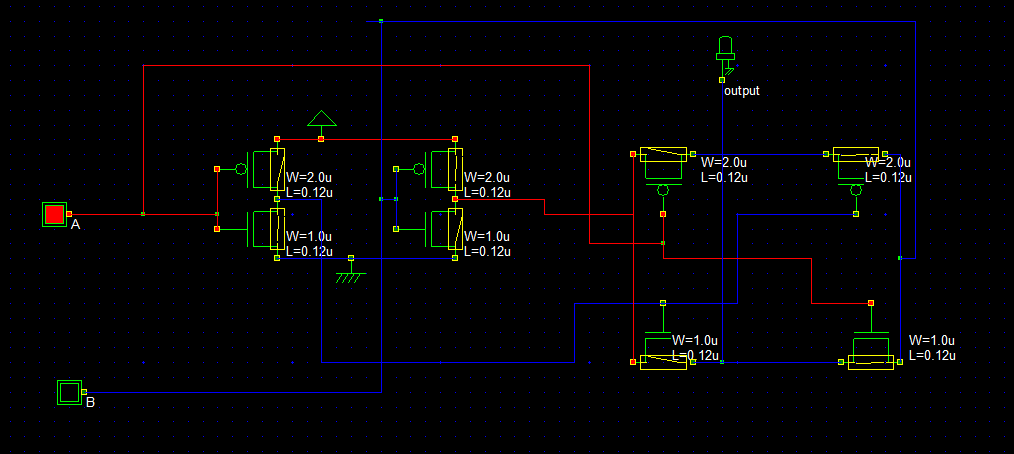
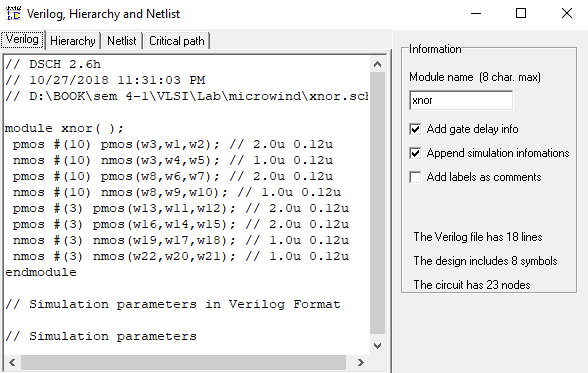


**Circuit Diagram**

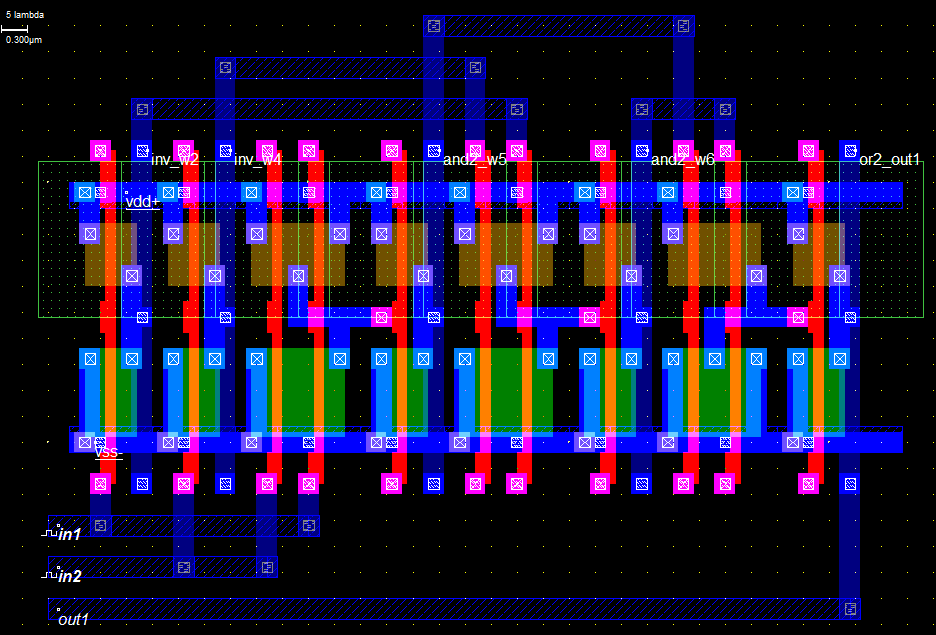
If two input is ‘1’ then the diagram is,

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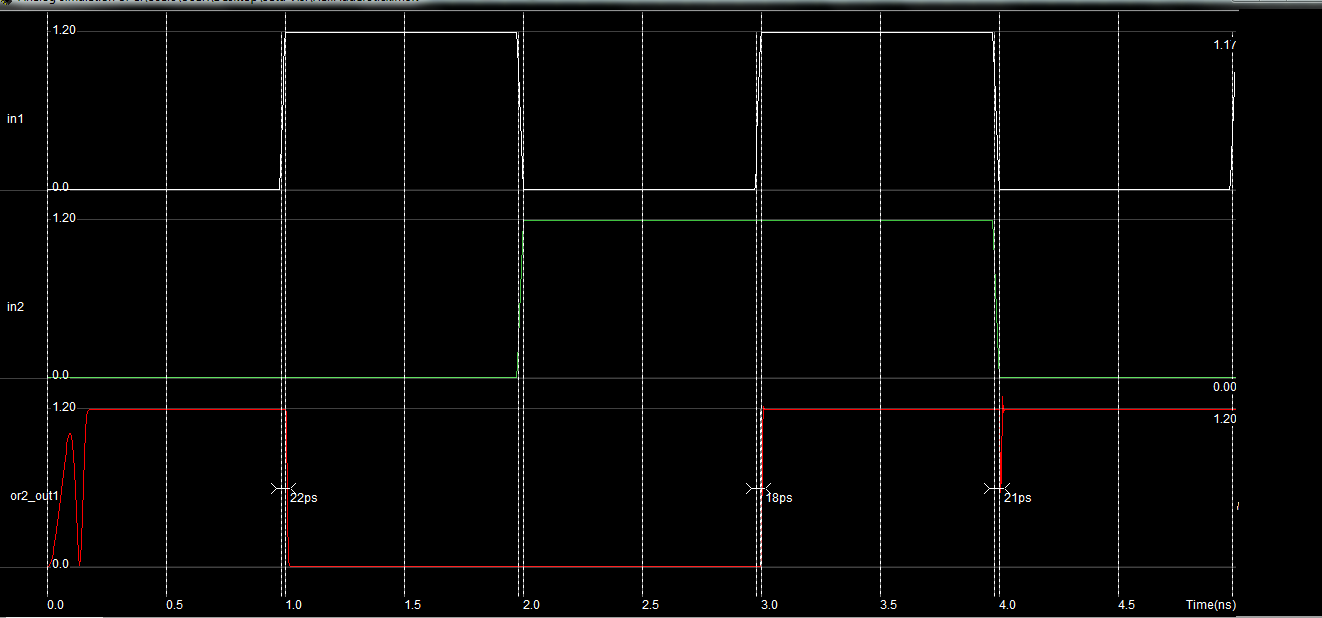
IF one input is ‘1’ and other is ‘0’, then

**Verilog File**

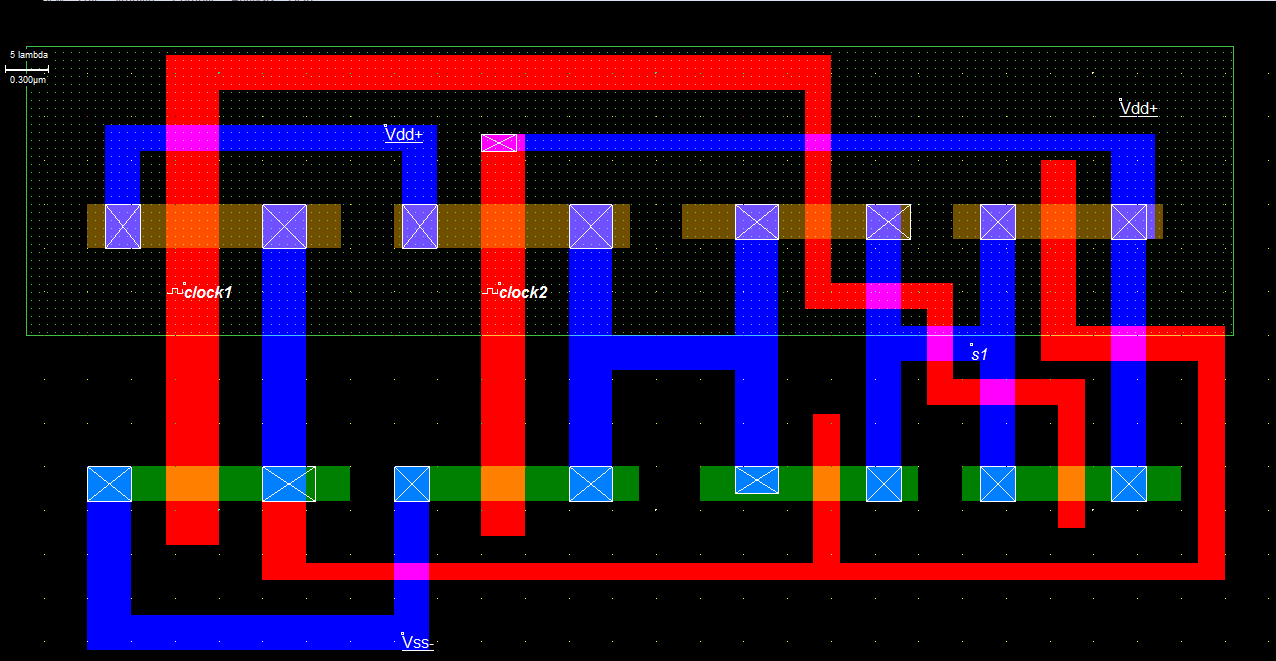
**Layout Diagram**



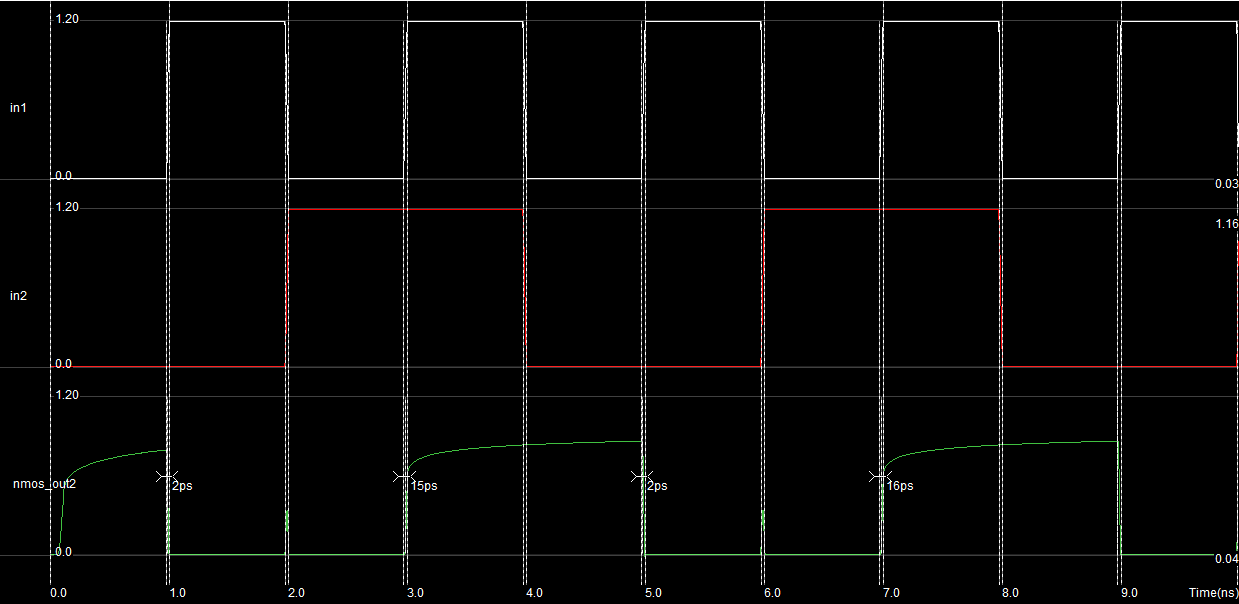
**Timing Diagram**

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**Stick Diagram**

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**Timing Diagram**

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**Discussion**

From the using and implementation of the xnor get, we can solve the many input with a single output problem. It can easily take input using the basic gate (AND,OR,NOT) and find the single output to calculate it.